



Design of a simplified reversible decimal adder in quantum computing based on excess-3 code

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Information loss occurs during the operation of classical computers, leading their operation processes to be irreversible. This information loss is accompanied by the release of heat from computers. However, quantum computers do not release such heat because their operation is basically reversible. Reversible quantum computation with Excess-3 code has attracted considerable attention recently. We suggest a design of a simplified decimal arithmetic circuit for reversible quantum computation based on Excess-3 code in this work. From rigorous tests for its overall computational processes with particular examples of addition, we have shown that this newly designed circuit gives exact computational results. By utilizing this circuit, more efficient quantum computing is possible.

INTRODUCTION

Thanks to recent remarkable developments in technology, it has become possible to fabricate nano-size electronic components and nano devices. Following this, rudimentary quantum computers that utilize novel characteristics of quantum mechanics have been realized. We expect the advent of highly efficient commercial quantum computers within a few decades. The ability of such quantum computers is expected to be significantly more powerful than that of existing ones. Quantum effects are very different from classical ones and emerge conspicuously as the size of electronic elements become smaller than the Fermi wavelength. When the size of a circuit's element approaches atomic scale, we cannot neglect quantum effects [1] while classical theory of electronics is no longer available in that situation. Such novel quantum effects can be applied to quantum information science such as quantum computation, quantum communication, and quantum cryptography. In particular, quantum computation implements special properties of quantum mechanics, which are superposition and entanglement.

During the operation of classical computers, they release a significant amount of heat because their operating processes are fundamentally irreversible. The cause of classical computers' irreversibility is that their operation processes are accompanied by information loss. According to Landauer's principle, a logic circuit generates heat when there is information loss in its computing processes [2]. The amount of heat released when one bit of information is erased in a computational operation is $k_B T \ln 2$ where k_B is Boltzmann's constant and T is the absolute temperature. As the circuit for a classical computer becomes complicated, the heat that it releases increases.

However, the circuits for quantum computation do not release such

heat because reversible arithmetic operation is adopted. Because there is no energy dissipation relevant to the information loss in the case of reversible computation, quantum computers consume very low electric power. From the test of Landauer's principle, Bennett showed the possibility of designing quantum computers adopted a general-purpose reversible algorithm [3].

Because decimal numbers are not always exactly represented by binary ones, errors occur when converting the decimal code to the binary one [4,5]. Due to this, we need decimal code in the computation. A most well-known decimal code is BCD (binary coded decimal) code [6]. Another noteworthy decimal code is Excess-3 code. We can obtain each codeword of Excess-3 code by adding 0011 from equivalent codeword of BCD. A particular characteristic of Excess-3 code is that it has the property of self-complementation, i.e., the codewords that correspond to the characters from 0 to 4 (in decimal) are compliments of the codewords from 9 to 5, consecutively. We can easily convert this code to other ones such as BCD or binary code using specially fabricated code-converters [7,8]. Owing to these properties, Excess-3 code can be conveniently implemented in computational processes [9-12]. The application of Excess-3 code in quantum computation first appears in Ref. [13] as far as we know. We designed a reversible adder for quantum computation using Excess-3 code in a previous paper [11] and in a subsequent work developed it [12]. In this work, we will propose a more simplified logic circuit for a decimal adder that operates using Excess-3 code. This may provide an efficient reversible computing resource that can be used in quantum computing.

DESIGN OF A SIMPLIFIED REVERSIBLE ADDER

Reducing the number of garbage outputs as well as minimizing quantum costs is the primary interest when designing quantum logic circuits [14]. To simplify the circuit, one needs to lower the number of garbage outputs in the circuit. We propose a simplified reversible logic circuit of a decimal adder that adopts Excess-3 code in this section. For quantum

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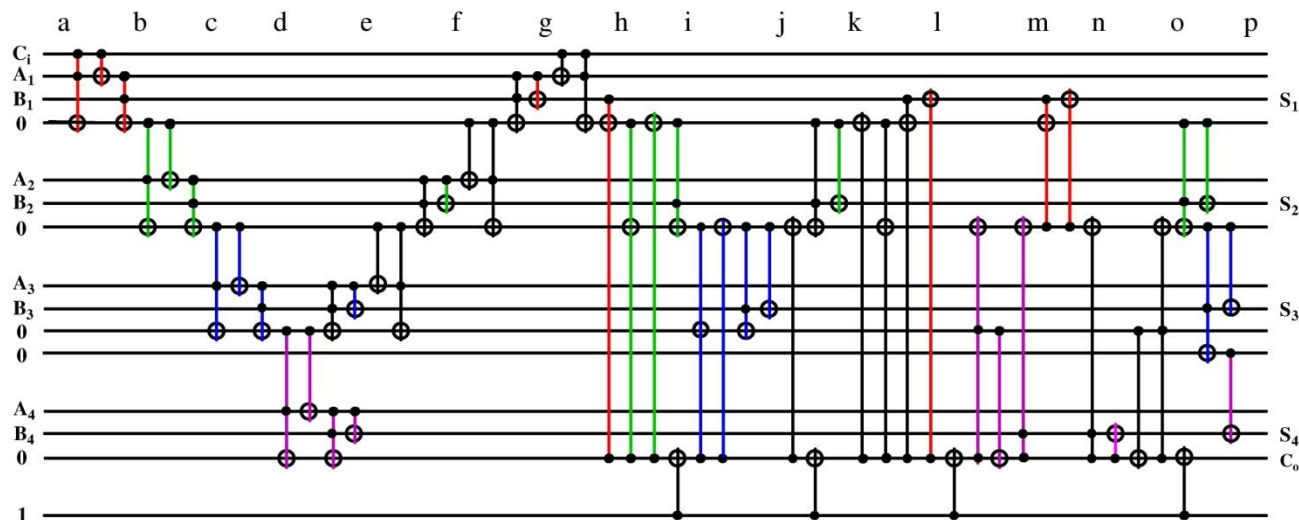


Figure 1 A simplified decimal adder in quantum computation, which operates using Excess-3 code

Table 1 Detailed data for the change of each qubit value with time for the circuit given in Fig. 1 in the case of the adding operation given in Example 1.

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	
C ₁	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S ₁
A ₁	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
B ₁	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1	
0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	
A ₂	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	S ₂
B ₂	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	1	1	1	0	0	0	0	1	0	0	1	1	0	0	
A ₃	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	
B ₃	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	S ₃
0	0	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
A ₄	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
B ₄	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	S ₄ C ₀
0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Table 2 This table represents the same information as table 1, but in the case of the adding operation given in Example 2.

	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p	
C ₁	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S ₁
A ₁	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
B ₁	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
A ₂	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	S ₂
B ₂	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	0	0	
A ₃	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	
B ₃	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	S ₃
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
A ₄	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
B ₄	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	S ₄ C ₀
0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0	1	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

logic circuits which are reversible, input qubits become output qubits at a later time. Due to this, the number of output qubits is always the same as input ones, enabling us to carry out reversible quantum computation. For the flowchart of such reversible computation for decimal adders based on Excess-3 code, and for the circuits of reversible quantum half and full adders, refer to Ref. [11] or [13].

By removing a garbage qubit line from the most recently designed circuit given in Ref. [12], we have simplified the arithmetic procedure of quantum computing. The circuit of Ref. [12] is composed of 16 operating lines. The 15th line among them, which is a garbage line, was removed when we designed our circuit in the present work. The details of that circuit are shown in Fig. 1. The role of the removed line has been taken over by another line which is the next line to B₂ line, which has an initial value of 0. After reuse of that garbage line for such a purpose, its value then recovers to what it had been before in order for the next use that was originally planned.

The circuit given in Fig. 1 has six garbage lines. Among them, the initial qubit value is 0 for the first five lines whereas that of the last garbage line is 1. It is easily confirmed by inspection that, from point 1 in Fig. 1, our circuit design is different from the one in Ref. [12]. Meanwhile the arithmetic results of the adding process for this adder are exact, this circuit has the fewest garbage lines among every circuit designed up to now in this field. This is the main development presented in this work.

TEST OF THE CIRCUIT WITH EXAMPLES OF COMPUTING OPERATION

To check whether the reversible adder works well, we consider two examples of simple computations:

- **Example 1:** First, let's consider an arithmetic evaluation $2+4=6$ (in Excess-3 code: $0101 + 0111 = 1001$) which output carry does not happen.
- **Example 2:** Now we will see an example that produces a carry as the result of computation. For such purpose, we regard $7+8=15$ ($1010 + 1011 = 0100\ 1000$).

For the purpose of simplicity, we have supposed that no carry has been received from the previous computational step, i.e., $C_i = 0$ for both of the above examples.

You can see from table 1 that the computing result of Excess-3 adder in the case of example 1 is $(S_4S_3S_2S_1) = (1001)$, while that of example 2 is $(S_4S_3S_2S_1) = (1000)$ with an output carry as shown in table 2. One can easily confirm that these results are exact. Hence, the simplified reversible adder works well, as expected.

CONCLUSION

Quantum states of qubits are fragile by the influence of the external noise or disturbance. According to the theory of decoherence, a quantum system can easily collapse to a classical one via its interaction with the external environment such as thermal photons which are ubiquitous. Hence, decoherence-induced errors may take place in the quantum computation, especially when an intricate computation is processed with many qubits. Such decoherence is known as the main obstacle in the development of a quantum computing algorithm. For this reason, the simplification of a computing circuit is important for the realization of controllable error-free quantum computers.

As noted earlier, quantum logic circuits that perform quantum computation are reversible in general, whereas classical circuits operate under a non-reversible paradigm. Reversible circuits enable us to have high-level computation and data processing with low electricity

consumption. In this work, we have designed a useful circuit of a reversible decimal adder that works using Excess-3 code, as shown in Fig. 1. This is the major development of the present work. By comparing Fig. 1 with the circuits given in previous papers, we can confirm that the circuit proposed in this work is the most simplified one among the circuits devised in this field up to now.

The operation lines of the previously designed most up-to-date circuit (Ref. [12]) with the same purpose are 16, where seven among them are garbage lines. However, from Fig. 1, we see that our updated computing circuit has 15 operation lines. This simplification has been enabled by reducing a garbage line from the circuit in Ref. [12]. The role of the removed garbage line has been undertaken by another garbage line which is the line just after the B₂ line. To justify that our improved circuit works well, we have checked it for two examples of adding processes. From this, we have confirmed that the results of computing processes for our circuit are exact. More efficient quantum computation can be possible by taking advantage of this improved logic circuit.

REFERENCES

1. J. R. Choi, Squeezing effects applied in nonclassical superposition states for quantum nanoelectronic circuits. *Nano Convergence*, vol. 4, 17 (2017).
2. R. Landauer, Irreversibility and heat generation in the computing process. *IBM J. Res. Develop.*, vol. 5, no. 3, 183-191 (1961).
3. C. H. Bennett, Logical reversibility of computation. *IBM J. Res. Develop.*, vol. 17, no. 6, 525-532 (1973).
4. H. Thapliyal, H. R. Arabnia, R. Bajpai, K. K. Sharma, Partial reversible gates (PRG) for reversible BCD arithmetic. Proceedings of the 2007 International Conference on Computer Design (CDES'07), Las Vegas, USA, June 2007, pp. 90-91 (CSREA Press).
5. H. Thapliyal, S. Kotiyal, M. B. Srinivas, Novel BCD adders and their reversible logic implementation for IEEE 754r format, Proceedings of the 19th IEEE/ACM International Conference on VLSI Design (VLSI Design 2006), Hyderabad, India, 2006, pp. 387-392. IEEE Computer Society Press.
6. H. Pelka, Computation with BCD (Binary-Coded-Decimal) numbers. *Elektroniker*, vol. 15, el14-el20 (1976).
7. M. Gandhi S, J. Devishree, Design of reversible code converters for quantum computer based systems, IJCA Proceedings on Amrita International Conference of Women in Computing (AICWIC'13), Amrita University Coimbatore, India, January 2013, pp. 27-30.
8. Rahman, Md. A. Habib, A. N. Bahar, Z. Rahman, Novel design of BCD to Excess-3 code converter in quantum dots cellular automata (QCA). *Global J. Res. Eng. F: Electr. Electron. Eng.*, vol. 14, no. 4, 7-11 (2014).
9. V. V. Blatov, A. A. Chudov, Binary-decimal adder-subtractors. *Instrum. Exp. Tech.*, vol. 21, no. 5, pt. 1, 1260-1264 (1978).
10. V. S. P. Nayak, N. Ramchander, R. S. Reddy, T. Marandi, Analysis and design of reversible excess-3 adder and subtractor. IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology, Bangalore, India, May 2016, pp. 397-400.
11. J. R. Choi, Optimal logic circuit design for reversible quantum computation based on Excess-3 code. *Discovery*, vol. 52, no. 246, 1483-1493 (2016).
12. J. R. Choi, J. N. Song, Improved quantum logic circuit for reversible quantum computation. *Discovery*, vol. 53, no. 260, 448-4533 (2017).

13. K. H. Yeon, J. R. Choi, D. Kim, M.-S. Kim, M. Maamache, Reversible quantum computation using Excess-3 code. *AIP Conf. Proc.*, vol. 1444, 310-313 (2012).
14. M. Mohammadi, M. Eshghi, M. Haghparast, A. Bahrololoom, Design and optimization of reversible BCD Adder/Subtractor circuit for quantum and nanotechnology based systems. *World Appl. Sci. J.*, vol. 4, no. 6, 787-792 (2008).

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Abbreviations: BCD - binary coded decimal

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